W-BAND GaAs MESFET FREQUENCY DOUBLER*

by

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ABSTRACT

A monolithic W-band frequency doubler has been developed using submicron gate length GaAs MESFETs fabricated on ion implanted material. The frequency doubler provides a power output of over 4.0 mW at 94 GHz with an input drive of 70 mW at 47 GHz. To our knowledge this is the first report of a MESFET frequency doubler operating at W-band.

INTRODUCTION

Recent progress in the development of GaAs MESFETs and MODFETs has generated intense interest in the extension of FET based devices and monolithic ICs to W-band frequencies. Of particular interest is the development of monolithically integrable W-band sources with power output sufficient to supply local oscillator drive to mixers. Reports of GaAs MESFETs and MODFETs operating in a fundamental frequency mode indicate that oscillators with 0.1 mW output at 110 GHz [1] and low gain amplifiers with 3.4 mW output at 94 GHz [2] can be achieved. However, frequency stability of the source is also a consideration and frequency stable oscillators are more easily fabricated at lower frequencies where FETs provide higher gain and dielectric resonators of reasonable size are readily available. An alternative to the fundamental frequency source is a lower frequency stabilized oscillator followed by a frequency doubler. Reports on GaAs monolithic power amplifiers [3] indicate 1-200mW output is possible in the 40-50 GHz range. This sets a limit for reasonable input power levels that can be expected for a monolithic W-band doubler.

In this paper we report on results achieved with a monolithic GaAs MESFET frequency doubler for W-band. The monolithic doubler incorporates an all-FET approach and therefore is more readily integrable with other FET-based monolithic circuitry than a monolithic varactor doubler [4]. Although high output conversion efficiency has been reported for a W-band varactor doubler in waveguide mounting [5], the output power is relatively low. Higher output power varactor doublers have been reported but with reduced conversion efficiency [6]. These conversion efficiencies would certainly be lower in a microstrip version of a varactor doubler. MESFET doublers have been demonstrated at frequencies up to 45 GHz [7,8] but to our knowledge this is the first report of a MESFET doubler operating at W-band.

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CIRCUIT DESIGN AND MODELING

The doubler design uses a balanced configuration for cancellation of odd harmonics similar to the approach described by Stancliff [4] except that a single gate FET is used in our designs. Two 0.35 x 300 micron single gate ion implanted FETs are used for the active elements. A virtual ground for the second harmonic is provided at the source of the balanced pair by on-chip quarter-wave stubs connected to the source of each device. Output matching is done with a quarter-wave transformer. The complete doubler chip is shown in Figure 1. Input matching, output matching, and the quarter-wave stubs for the second harmonic virtual ground at the sources are all provided on a .96 x .72 x .1 mm^3 chip. Use of monolithic integration is the key to implementation of an FET doubler at W-band since parasitics introduced in hybrid construction would preclude proper operation of the doubler. The doubler design was developed with the aid of a PC compatible version of SPICE to simulate doubler operation. A diagram of the circuit used in the simulation is shown in Figure 2. All circuit components except the quarter-wave transformer on the output were simulated by lumped elements due to limitations on the number of transmission lines that could be handled by the program. In the circuit implementation, inductors are replaced by high impedance transmission lines of appropriate length. Doubler operation was simulated running SPICE in the time response mode for a length of time sufficient to allow the decay of start up transients. Then, a Fourier analysis of the output was performed to determine the doubler output. Some optimization of the output matching components was done using experimental design techniques.

Two modes of operation are possible in MESFET frequency doublers:

- The V_{gs}=0 mode where the output voltage is nonlinear and the optimum load is a relatively high impedance.

o The $V_{gs}=-V_T$ mode where the output current is non-linear and the optimum load is a relatively low impedance.

Designs were developed for both modes of operation. The $V_g=-V_T$ mode offers high dc to RF conversion efficiency but relatively low RF conversion efficiency. On the other hand, the $V_g=0$ mode provides better RF conversion efficiency while sacrificing dc to RF efficiency. The difference in conversion efficiency is due, in large part, to the device transconductance which is lower near V_T than at $V_{gs}=0$. Figure 3 shows calculated power output vs power input for optimized designs in the two operating modes. A $V_g=0$ design is clearly superior in conversion efficiency. The model predicts that output power in excess of 10 mW can be achieved with 200 mW of input drive. Simulation results were based on typical device parameters for our submicron gate length ion implanted MESFETs. Higher transconductance devices such as MESFETs fabricated on epitaxial material or MODFETs will increase the output power and conversion efficiency.

IC FABRICATION

The doubler IC was fabricated using a hybrid lithography process consisting of e-beam direct-write for the mesa, ohmic, and gate levels, and contact optical lithography for defining the microstrip circuitry, capacitors, and air bridge interconnections. LEC substrate material with a 6 x 10^{12} cm^{-2}, 120 KeV silicon implant was used to form the channel layer. The material is furnace annealed at 850°C with a silicon nitride cap to activate the implant. The FETs in the doubler are 0.35 x 300 micron gate devices with six 50 micron gate fingers and interdigital source and drain contacts. A typical dc drain I-V for these devices is shown in Figure 4. These devices have a peak transconductance of 140 mS/mm and a threshold voltage of approximately -2.5 volts. Provisions for on-chip modifications to the input matching networks and the quarter-wave stubs connected to the source pads of the devices were included in the IC design. The RF results reported are for chips with no modification of the input matching networks. The quarter-wave stubs were modified for maximum power output at 94 GHz.

RF EVALUATION

RF evaluation of the FET doubler was done using a commercial 47 GHz waveguide Gunn oscillator for the source. To transition from waveguide to the push-pull microstrip input of the doubler chip, hybrid circuits etched on 5 mil CuFlon® and 5 mil sapphire were developed. Figure 5a shows a scaled diagram of the 47 to 94 GHz doubler module consisting of the doubler chip and the input and output hybrid interface circuits. At the input, the antipodal fin line circuit [9] provides a low loss (~0.5 dB) transition from standard U-band waveguide to a microstrip 50 ohm line on 5 mil CuFlon. The circuit fabricated on 5-mil sapphire includes a coupled line dc block and a 3 dB 180° hybrid circuit to provide the antiphase drive to the doubler chip. The fourth part of the 3 dB "rat race" is terminated with a 50 ohm chip resistor connected to an RF short which is provided by the radial open stub.

At the output a dc block and fin line transition designed for 94 GHz is fabricated on 3-mil CuFlon. The dc block dimensions are 12 mils long ($\lambda/4$) with a strip width and spacing of 0.7 mil and 0.4 mil respectively. The insertion loss for the dc block and transition combination is about 1 dB at 94 GHz. Figure 5b shows the actual module housed in the 47/94 GHz waveguide fixture.

For maximum output power the bias voltage used on the drain and gate was adjusted to 2.2V and 0V respectively. Figure 6 shows the resulting output power characteristic at 94 GHz versus the input power at 47 GHz. With an input drive level of 70 mW an output power of over 4.0 mW at 94 GHz is achieved. These power levels are referred to the input and output ports of the doubler chip, i.e., fixture losses have been taken into account. Although in our experiments the drive level was limited to 70 mW, it is seen in the curve of Figure 6 that greater power can be expected at higher input drives. Finally, Figure 7 shows the 94 GHz spectrum analyzer trace of the doubler output.

CONCLUSIONS

A GaAs MESFET based monolithic frequency doubler with 4.0 mW output at 5 percent conversion efficiency has been demonstrated in W-band. The use of monolithic integration is a key ingredient in the development of such a circuit due to reduced parasitics. The doubler described uses 0.35 x 300 micron gate ion implanted FETs for the active elements. In the future, the use of improved output matching networks and shorter gate length devices fabricated on epitaxially grown MESFET or MODFET material will result in higher power output and improved conversion efficiency.

ACKNOWLEDGEMENT

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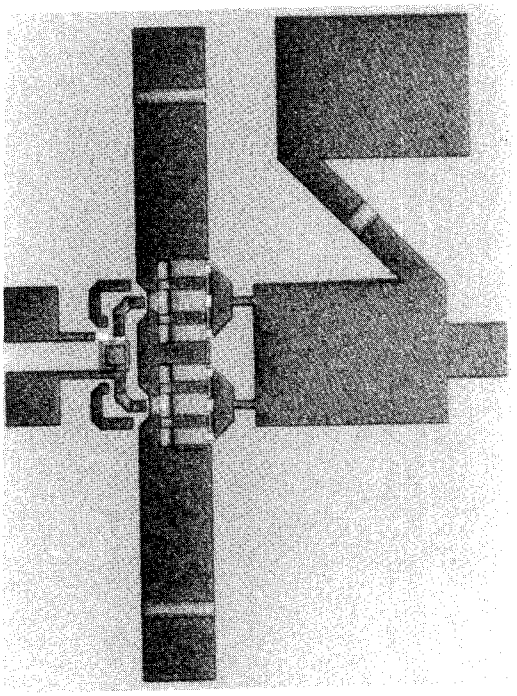

Figure 1. Monolithic W-Band Doubler Chip.

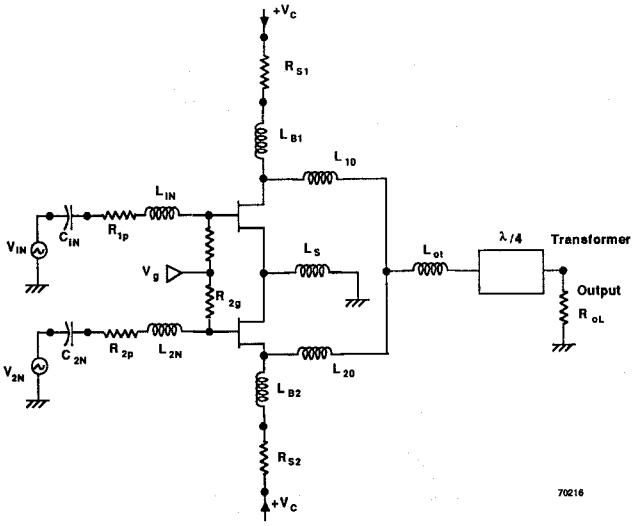

Figure 2. Balanced Doubler Circuit Used in SPICE Simulation.

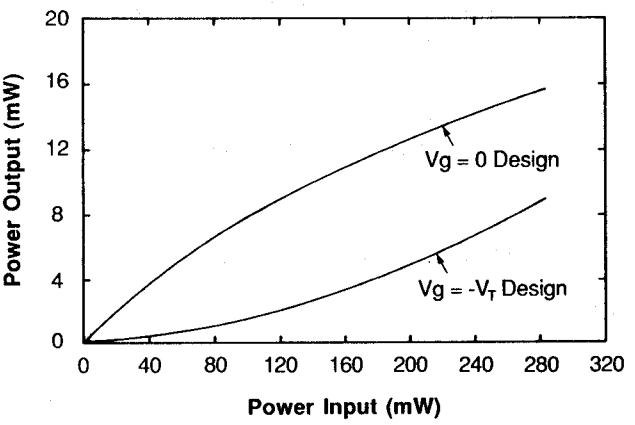

Figure 3. Doubler Power Output vs Input Calculated Using SPICE.

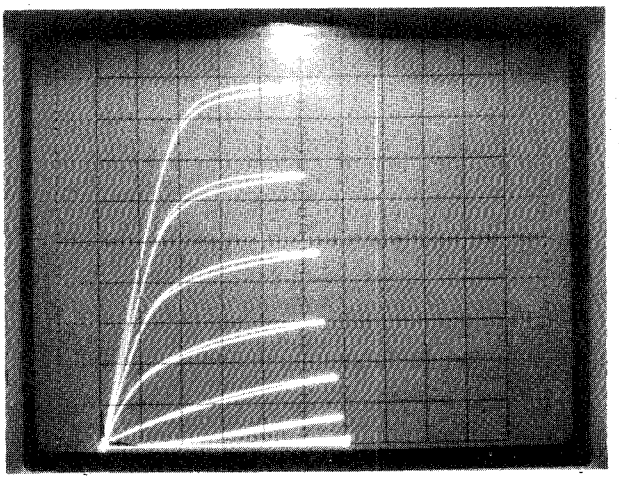

Figure 4. DC Drain IV of 0.35 x 300 Micron Gate FET Used in Doubler. [Vert: I_d = 10 mA/div; Horiz: V_d = .5V/div; Step Size:V_g = .5V]

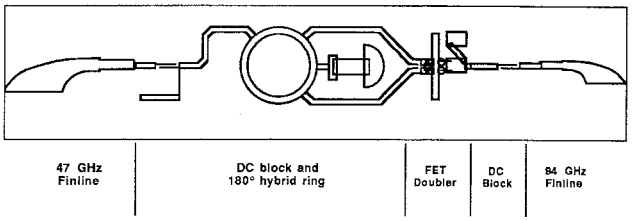

Figure 5a. Overall View of the 47-to-94 GHz Frequency Doubler Circuit.

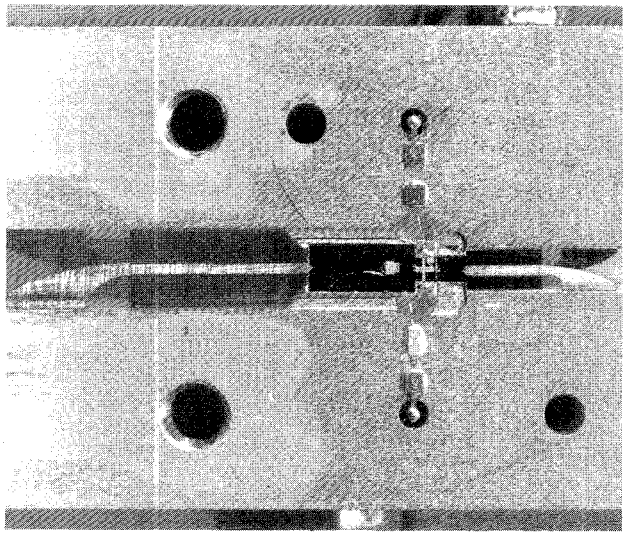

Figure 5b. Photograph of Doubler Chip in Test Fixture.

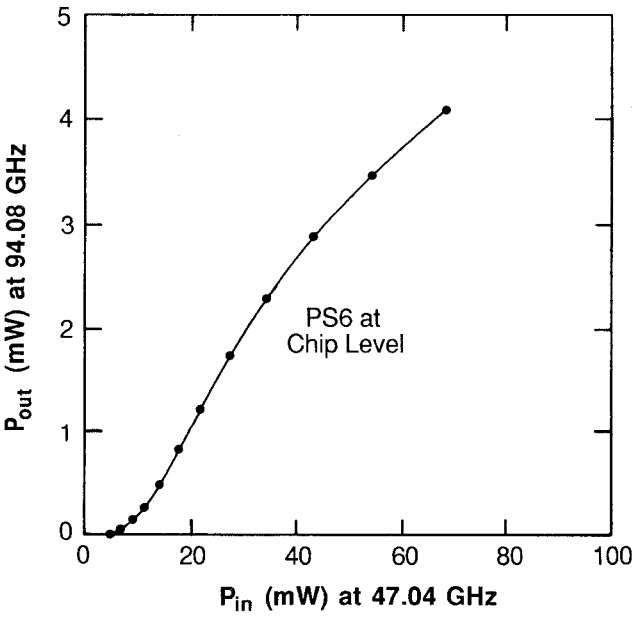

Figure 6. Chip Level Experimental Data for Doubler.

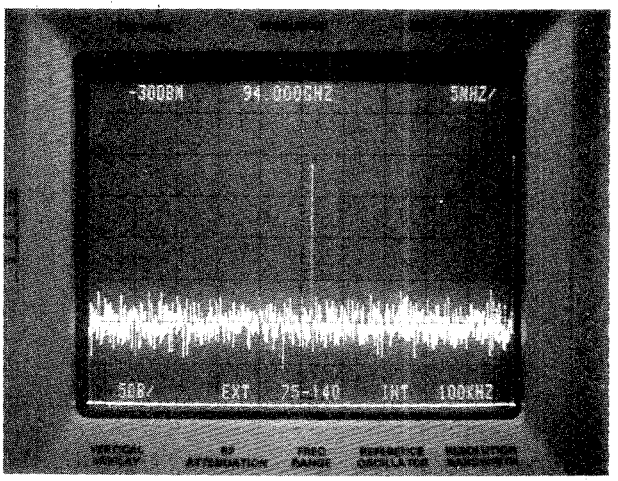

Figure 7. Spectrum of Doubler Output.